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Magnetic-Bubble Conservative Logic

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Among integrated-circuit devices, magnetic bubbles are a particularly interesting candidate to implement the Fredkin gate and conservative logic. The magnetostatic repulsion of magnetic bubbles simulates the bouncing-ball model of conservative logic.

1. MEMORY PRODUCTS AND LOGIC POTENTIALS

Since 1977, bubble memory modules (Chester, 1980) have been marketed by several companies (INTEL, National Semiconductors, Fujitsu, Hitachi, NEC, etc.). The largest commercial bubble memory chip at present (Chester, 1980) contains one million bits, with on-chip read and write as well as selection, detection, and redundancy functions. Four-million-bit memory chips are expected in 1982, and density improvement is expected to remain at a better pace than that of semiconductors. Bubbles exceed semiconductors in density and in chip capacity by about 10 times mainly due to the intrinsically simpler device structures (one or two critical lithography levels for memory cells and one additional level for logic gates). Bubble bits are intrinsically in data streams, natural for parallel and pipelined constructs. Moreover, the data flows and gate functions are all synchronized to a common drive (hence self-clocked). The signals in the form of bubbles are replenished in energy and renormalized during each step of bit movement (i.e., every clock cycle). The abundance of bits, data streaming, self-clocking, and signal renormalization appear to be unique advantages of bubble logic (Chang, 1975; Chen and Chang, 1978).

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The major disadvantages are slow speed (0.1 MHz data rate in commercial chips, but 10 MHz data rate in experimental devices) and geometrical constraints (stepwise movement of bubbles in a single plane). However, the regular structures to realize parallel and pipelined chip architectures such as systolic arrays or programmable logic arrays not only achieve speed improvement but also alleviate geometrical constraints (Chang, 1981).

2. CONSERVATIVE AND REVERSIBLE LOGIC

Bubbles must be created and destroyed deliberately, but not as a natural consequence of performing memory or logic function. Thus the term "conservative logic" has been in use since the early days of bubble logic study. In fact, conjugate gates (e.g., AND/OR) must be constructed since individual logic functions such as AND do not conserve bubbles (i.e., there is discrepancy in the numbers of bubbles at the input and the output). However, the term "conservative logic" as used by Fredkin and colleagues (Fredkin and Toffoli, 1981) requires logic elements to satisfy several essential conditions: (1) identity of information transmission and storage, (2) reversible operation (exchangeable inputs and outputs), (3) conservation of bits (i.e., no conversion of ONES to ZEROs, or vice versa); etc. While these requirements can be satisfied by the intrinsic properties of bubbles as we shall show in the next section, the second requirement was not satisfied by the "conservative logic" as described in early bubble literature (Chang, 1975; Chen and Chang, 1978).

The pursuit of conservative logic devices by Fredkin and Toffoli is aimed at constructing "zero-power' sequential circuits. At the conceptual level, they have evolved stylized axioms and abstract models to facilitate the design of complex computing machines. However, at the physical level, ideal elastic balls colliding with one another and steered by suitable guards are used to demonstrate how conservative logic elements can be constructed.

It appears that among integrated-circuit solid-state devices, magnetic bubbles with their magnetostatic repulsion phenomenon come closest to ideal elastic balls colliding with each other. In view of their high density, moderately high speed, and low (but not zero) power, it is reasonable to consider bubbles as a candidate to implement the reversible conservative logic.

3. BUBBLE FREDKIN GATE

The Fredkin gate is depicted and defined in Figure 1. The control data stream (u) steers the input data streams (x_1 and x_2) into the output data

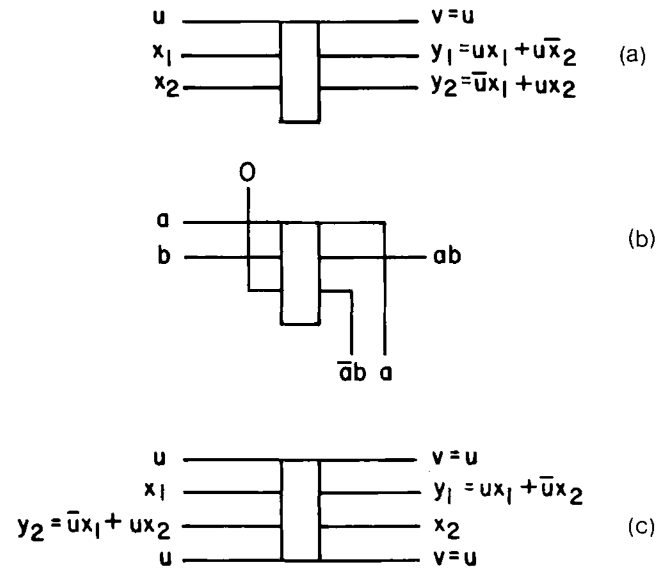

Fig. 1. Behavior of the Fredkin gate (a) with unconstrained inputs, (b) with x_2 constrained to the value 0, thus realizing the AND function, (c) dual-control gate.

streams (y_1 and y_2). Since logic is performed by redirecting data streams rather than changing ONE's to ZERO's or vice versa, the logic is conservative. From $y_1 = ux_1 + ux_2$ and $y_2 = ux_1 + ux_2$, it can be shown that $x_1 = uy_1 + uy_2$ and $x_2 = uy_1 + uy_2$. Hence, the gate is reversible. Moreover, the Fredkin gate is universal; i.e., other logic gates can be derived from it. Figure 1b illustrates how an AND gate is realized.

If the control is to be exercised by the magnetostatic Coulomb force of a bubble, a single control stream cannot exert the same force on both the near and far data streams. It is more practical to use two identical control streams equally spaced from the two data streams (see Figure 1c). But, the dual-control input requires that the outputs be duplicated (hence no longer conservative) to give subsequent dual control. This dilemma could be avoided by steering the single control stream close to the two data streams successively. Crossover and delay circuits will be needed in the implementation. We shall not go into the detailed circuitry here.

In Figure 2, a magnetic-bubble Fredkin gate is described. The block diagram in Figure 2a uses squares to represent bit positions, and arrows propagation paths. A unit delay is incurred between adjacent bit positions. Interaction between the control and data streams occurs at the two locations marked *I*. The two squares in the center serve as buffer positions such that

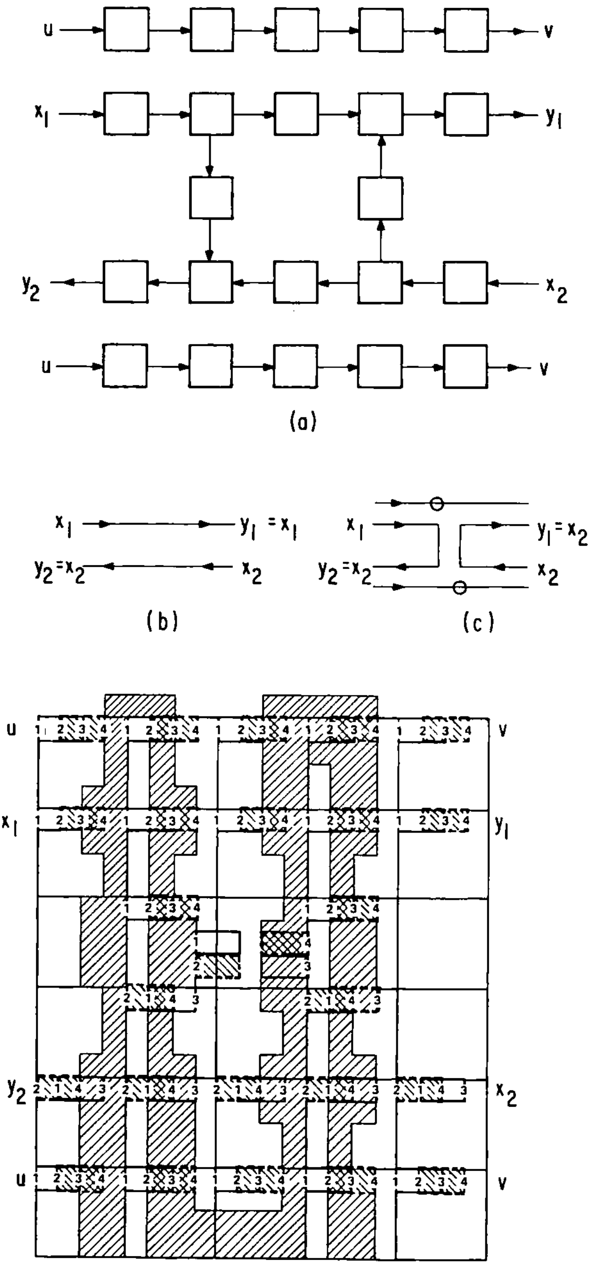

Fig. 2. Bubble implementation of Fredkin gate. (a) Block diagram with each square representing one bit position. (b) Data flow in the absence of control bubbles. (c) Data flow in the presence of control bubbles. (d) Three patterned metallic layers on a magnetic garnet film to implement the device.

when the control streams alter the data stream paths, there will be no gap or overlapping of bits. Also note that the control streams are not affected by the data streams. In Figures 2b and 2c are shown, respectively, the data paths in the absence and presence of control bubbles.

Figure 2d shows the design pattern for a bubble device. The unshaded and shaded rectangles are the holes in the first- and second-layer propagation conductors, respectively, and the shaded meandering conductor is for control. The propagation/memory devices (i.e., shift registers) along with other ancillary components for a memory chip have been designed, fabricated, and tested by Bobeck et al. (1979). To explain the propagation action, we observe that the holes distort the uniform current flow to concentrate current at the two ends, and create an attractive pole at one end and a repulsive pole at the other. With holes in the two sheets properly displaced and currents in the two sheets alternating and properly time-phased, an alternately attractive/repulsive pole train is created to propagate bubbles. The superimposed conductor, when conducting current, will elongate the control bubbles (if present) to force data bubbles into the buffer positions. Although our design has not yet been verified experimentally, a similar gate (specifically, an AND/OR gate) in permalloy patterns has been demonstrated by Nelson (1975).

4. PROSPECTS

Commercial bubble devices have 10^6 bits/cm^2 density, (2 μm bubble diameter) 10 μs unit propagation delay (0.1 MHz data rate), and several microwatts per bit power dissipation. Experimental devices offer greater than 10^7 bits/cm^2 density and higher than 5 MHz data rate. With the use of flux-closure structures to reduce drive field and current, less than 1 μW per bit power is expected. Speaking of intrinsic physical limits, Keyes (1971) made heuristic analysis and estimated that the bubble diameter could be as small as 100 Å (smallest ever observed experimentally is 800 Å), the energy to move a bubble about 10^{-8} erg, the unit propagation delay 10 ns, and the per-bit power dissipation 0.01 μW.

Bubble logic capability in general could alleviate interconnection problems caused by different media for memory and logic, and improve performance by intermingling memory and logic to reduce unnecessary data traffic. The steady improvement in manufacturing capability will provide larger and larger chip capacity. Concepts such as conservative logic, systolic array, programmable logic array make it worthwhile to explore new avenues of integrated memory/logic systems for bubble technology.

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